

Digital Logic Design Lab

Department: Computer Science and Engineering

Semester: Spring-2017

Course Code: CSE-345

Course Title: Digital Logic Design

Post-Lab Work: 06

Title: Multiplexer and its use in

Combinational Logic Implementation

**Submitted By :**

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**Objectives:**

1. To implement and test a 4-to-1 line multiplexer with active-LOW enable input using random gates.
2. To implement and test combinational logic function using IC 74151 (8-to-1 line multiplexer with active-LOW enable input).

**Answers to the Post Lab-Report Questions:**

**Answer 1:**

Implementing and testing a 4-to-1 line multiplexer with active-LOW enable input using random gates:

|  |  |  |
| --- | --- | --- |
| Inputs | Pre-lab Outputs | Experimental Outputs |
| E |  |  |
| 0 0 0 |  |  |
| 0 0 1 |  |  |
| 0 1 0 |  |  |
| 0 1 1 |  |  |
| 1 0 0 | 0 | 0 |
| 1 0 1 | 0 | 0 |
| 1 1 0 | 0 | 0 |
| 1 1 1 | 0 | 0 |

**Comment:** There is no difference between experimental and pre-lab results.

**Implementing and testing combinational logic function using IC 74151 (8-to-1 lines multiplexer with active-LOW enable input):**

|  |  |  |
| --- | --- | --- |
| Inputs | Pre-lab Outputs | Experimental Outputs |
| A B C D | F | F |
| 0 0 0 0 | 1 | 1 |
| 0 0 0 1 | 0 | 0 |
| 0 0 1 0 | 0 | 0 |
| 0 0 1 1 | 1 | 1 |
| 0 1 0 0 | 1 | 1 |
| 0 1 0 1 | 0 | 0 |
| 0 1 1 0 | 1 | 1 |
| 0 1 1 1 | 0 | 0 |
| 1 0 0 0 | 1 | 1 |
| 1 0 0 1 | 0 | 0 |
| 1 0 1 0 | 0 | 0 |
| 1 0 1 1 | 1 | 1 |
| 1 1 0 0 | 0 | 0 |
| 1 1 0 1 | 1 | 1 |
| 1 1 1 0 | 0 | 0 |
| 1 1 1 1 | 1 | 1 |

**Comment:** There is no difference between experimental and pre-lab results.

**Answer 2:**

**Structural Verilog code for the logic diagram for a 4-to-1 line multiplexer with active-LOW enable :**

*module expt6\_1 (input E, A1, A0, I0, I1, I2, I3, output O);*

*wire w1, w2, w3, w4;*

*and g1(w1, ~E,~A1,~A0,I0),*

*g2(w2, ~E,~A1,A0,I1),*

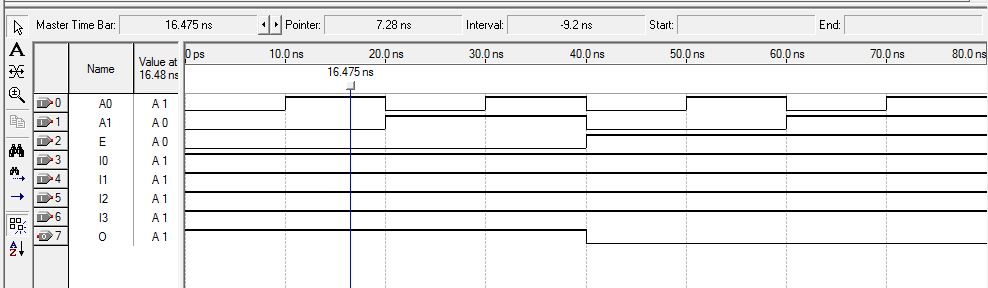
*g3(w3, ~E,A1,~A0,I2),*

*g4(w4, ~E,A1,A0,I3);*

*or g5(O, w1,w2,w3,w4);*

*endmodule*

**Simulation of the structural Verilog code:**



**Answer 3:**

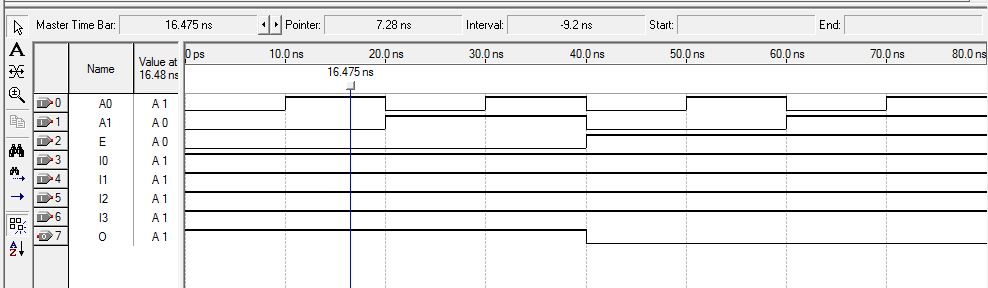
**Behavioral Verilog code for a 4-to-1 line multiplexer with active-LOW enable input :**

*module expt6\_2(output O, input E,A1,A0,I0,I1,I2,I3);*

*assign O= (I0&~E&~A1&~A0)| (I1&~E&~A1&A0) | (I2&~E&A1&~A0) | (I3&~E&A1&A0);*

*endmodule*

**Simulation of the behavioral Verilog code:**



**Conclusion:**

After completing this experiment, we can learn how to implement a 4-to-1 line multiplexer with active-LOW enable input , and also implement the combinational Logic functions using IC 74151(8-to-1 line multiplexer with active-LOW outputs). We also learn to implement the simulation of these multiplexer circuits by using structural verilog code in Quartus II software.